## REMARKS

Claims 1-15 are now pending in the application. Applicant has amended Claim 2 to include changing a value of the output means synchronously with the standard clock and within a predetermined number of cycles of the standard clock. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

### SPECIFICATION

The specification stands objected to for certain informalities. Applicant has amended the specification according to the Examiner's suggestions. More specifically, Applicant has amended the title so that it is more descriptive. Therefore, reconsideration and withdrawal of this objection are respectfully requested.

### REJECTION UNDER 35 U.S.C. § 112

Claims 1-15 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention. This rejection is respectfully traversed.

Referring to Claims 1 and 2, Applicant has amended Claims 1 and 2 to include outputting "signal information from the control processor" in order to provide proper antecedent basis. Applicant has amended Claims 1 and 2 to include "the control processor performs an operation according to signal information" in order to further clarify operation of the control processor. Applicant has also amended Claim 1 to include changing a value of the output means "within one cycle of the standard clock" in

order to further clarify operation of the output means. Applicant believes the rejection of Claims 1 and 2 under 35 U.S.C. § 112, second paragraph, is now moot.

Claims 3-7 and 9-15 depend directly or indirectly from Claim 1. Therefore, Applicant believes the rejection of Claims 3-7 and 9-15 under 35 U.S.C. § 112, second paragraph, is also now moot for the reasons cited above.

Referring to Claim 8, Applicant has amended Claim 8 to include waiting for "a value of the signal information" and "said control processor performs an operation according to the predetermined value" in order to provide proper antecedent basis. Applicant believes the rejection of Claim 8 under 35 U.S.C. § 112, second paragraph, is now moot.

**REJECTION UNDER 35 U.S.C. § 102**

Claims 1-6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Charles et al. (U.S. Pat. No. 5,790,842). This rejection is respectfully traversed.

Referring to Claim 1, Charles et al. do not show, teach, or suggest a control processor performing an operation according to signal information that is captured from an input means synchronously with a standard clock and a value of an output means is changed by the control processor within one cycle of the standard clock.

Charles et al. teach a set top box processing system that permits simultaneous utilization of two system clocks. The set top box processing system includes an ASIC processor and clock circuitry (col. 8, line 45). The clock circuitry allows elements of the set top box processing system such as a video decoder and an NTSC encoder to communicate with the ASIC processor while using different clocks (col. 18, line 42 and

See FIG. 5A). The video decoder and the NTSC encoder operate using a first clock and the ASIC processor operates using a second clock that is a non-integer multiple of the first clock (col. 20, line 66).

A synchronous phase detector generates an enable signal based on the first and second clocks (col. 19, line 3). The enable signal transitions high when both the first and second clocks transition high simultaneously. The ASIC processor utilizes clock frequency conversion hardware including flip-flops and multiplexers to allow the video decoder and the NTSC encoder to communicate with state-based logic in the ASIC processor (col. 20, line 17). The clock frequency conversion hardware converts the clock frequencies based on the first and second clocks and the enable signal (See FIG. 6A).

The state-based logic does not change a value that is output by the state-based logic within one cycle of the first clock (27MHz), as required by the claims. Signals are input to the ASIC processor from the video decoder according to the first clock. A multiplexer and a flip-flop convert the signals so that the signals correspond with the second clock (40.5MHz) before being input to the state-based logic (col. 20, line 24). As shown in FIG. 6B, a full cycle of the first clock occurs during the conversion of the signals between the first and second clocks. Multiple cycles of the first clock are then required for the state-based logic to process the signals.

Signals that correspond with the second clock are output by the state-based logic. Two flip-flops convert the signals output by the state-based logic so that the signals correspond with the first clock (col. 20, line 44). Numerous cycles of the first clock occur between signals being output by the video decoder and signals being

received by the NTSC encoder. Since the second clock is a non-integer multiple of the first clock, it is difficult to match the first and second clocks in a minimal number of cycles of the first clock. Therefore, independent clock conversion circuitry is required in the system taught by Charles et al.

Applicant teaches a program logic device that includes a control processor operating based on a high speed clock. The high speed clock is an integer multiple of a standard clock. The control processor receives an input signal synchronous with the standard clock, processes the input signal, and generates an output signal synchronous with the standard clock and within one cycle of the standard clock. Since the high speed clock is an integer multiple of the standard clock, the control processor may be programmed to generate the output signal synchronous with the standard clock and within one or more predetermined cycles of the standard clock. Therefore, unlike the system taught by Charles et al., independent clock conversion circuitry that delays processing of the input signal is not required.

Claims 3-15 depend directly or indirectly from Claim 1 and are allowable over Charles et al. for the same reasons.

Referring to Claim 2, Charles et al. do not show, teach, or suggest a control processor performing an operation according to a value of signal information that is captured from an input means synchronously with a standard clock and a value of an output means is changed by the control processor synchronously with the standard clock and within a predetermined number of cycles of the standard clock.

The arguments made above with respect to Claim 1 are equally applicable to Claim 2. Since the second clock is a non-integer multiple of the first clock, it is difficult

to synchronize the first and second clocks. Therefore, the system taught by Charles et al. requires independent clock conversion circuitry. A multiplexer and a flip-flop convert signals output by the video decoder so that the signals correspond with the second clock before being input to the state-based logic. Two flip-flops convert signals output by the state-based logic so that the signals correspond with the first clock.

Additionally, the state-based logic does not change a value that is output by the state-based logic synchronously with the first clock and within a predetermined number of cycles of the first clock, as required by the claims. Charles et al. are silent with respect to changing a value that is output by the state-based logic within a predetermined number of cycles of the first clock. Since the second clock is a non-integer multiple of the first clock, the signals output by the state-based logic may only be synchronous with the first clock when the cycle number is evenly divisible by the ratio between the second and first clocks.

On page 12, line 12 of the Application, Applicant teaches that there are some cases where it is inappropriate to define an output within one cycle of a standard clock. Therefore, Applicant teaches that the control processor may generate the output signal after a predetermined number of cycles of the standard clock. Unlike the clocks in the system taught by Charles et al., the high speed clock is an integer multiple of the standard clock. Therefore, the control processor is capable of generating the output signal synchronous with the standard clock and within any predetermined number of cycles of the standard clock.

**CONCLUSION**

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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